

IN THE UNITED STATES DESIGNATED OFFICE (DO/US)

In re: Hamilton, et al.

Attn: DO/US

International Appl. No.: PCT/GB2003/002599

International Filing Date: June 17, 2003

For: DIGITAL SYSTEM AND METHOD FOR TESTING

ANALOGUE AND MIXED SIGNAL CIRCUITS OR SYSTEMS

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**INFORMATION DISCLOSURE STATEMENT**

Sir:

At least some of the patents and publications listed on the attached PTO-1449 were cited in the above-referenced application and/or the International Search Report of corresponding International Application No. PCT/GB2003/002599. Copies of the Search Report and Examination Report are enclosed for the Examiner's convenience and consideration. In accordance with the Office waiver published July 11, 2003, copies of the cited U.S. patents and patent application publications are not enclosed. Applicant does enclose copies of any cited foreign patent documents and non-patent literature in accordance with 37 CFR 1.98(a)(2).

The Examiner may wish to consider the notations on the Search Report itself regarding the relevance of each item. It is requested that the Examiner consider these references and officially make them of record in accordance with the provisions of 37 C.F.R. § 1.97 and Section 609 of the MPEP. By submitting the listed documents, Applicant in no way makes any admission as to the prior art status of the listed documents, but is instead submitting the listed documents for the sake of full disclosure.

Respectfully submitted,

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(Revised 04/2003)

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 2

**Complete if Known**

Application Number	PCT/GB2003/002599
Filing Date	06/17/2003
First Named Inventor	Hamilton
Group Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	031749/286126

**U. S. PATENT DOCUMENTS**

Examiner Initials*	Cite No.	<u>Document Number</u> Number - Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages of Relevant Figures Appear
	1	US-5,694,356	12/02/1997	Wong et al.	
	2	US-5,745,409	04/28/1998	Wong et al.	
	3	US-5,748,124	05/05/1998	Rosenthal et al.	
	4	US-5,793,778	08/11/1998	Qureshi	
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**FOREIGN PATENT DOCUMENTS**

Examiner Initials	Cite No.	<u>Foreign Patent Document</u> Country Code - Number Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	English Language Translation Attached
	5	WO 98/55880	12/10/1998	Hamida et al.		

Examiner  
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Date  
Considered

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Substitute for form 1449/PTO (Revised 04/2003)  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)				<b>Complete if Known</b>	
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				First Named Inventor	Hamilton
				Group Art Unit	Unknown
				Examiner Name	Unknown
Sheet	2	of	2	Attorney Docket Number	031749/286126
<b>OTHER DOCUMENTS</b>					
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			English Language Translation Attached
	6	ZHENG ET AL.; <i>A Novel Test Generation Approach for Parametric Faults in Linear Analog Circuits</i> ; 14th IEEE VLSI Test Symposium; 1996; Pages 470-475 (XP-002265465)			
	7	SAAB ET AL.; <i>CRIS: A Test Cultivation Program for Sequential VLSI Circuits</i> ; IEEE; 1992; Pages 216-219			
	8	VAN SPAANDONK ET AL.; <i>Selecting Measurements to Test the Functional Behavior of Analog Circuits</i> ; Journal of Electronic Testing: Theory and Applications; 1996; Pages 9-18; Vol. 9; Kluwer Academic Publishers, The Netherlands (XP-000636621)			
	9	BALIVADA ET AL.; <i>A Unified Approach for Fault Simulation of Linear Mixed-Signal Circuits</i> ; Journal of Electronic Testing: Theory and Applications; 1996; Pages 29-41; Vol. 9; Kluwer Academic Publishers, The Netherlands (XP-000636623)			
	10	SOUDERS, ET AL.; <i>Accurate Frequency Response Determinations from Discrete Step Response Data</i> ; IEEE Transactions on Instrumentation and Measurement; June 1987; Pages 433-439; Vol. IM-36, No. 2			
	11	ECKERSALL, ET AL.; <i>Testing an Analogue Circuit Using a Complementary Signal Set</i> ; IEE Colloquium on "Testing Mixed Signal Circuits, 1992; Pages 5/1-5/6; Digest No. 1992/118			
	12	AL-QUTAYRI, ET AL.; <i>Go/no-go Testing of Analogue Macros</i> ; IEE Proceedings; August 1992; Pages 534-540; Vol. 139, No. 4			
	13	PAN, ET AL.; <i>Pseudorandom Testing for Mixed-Signal Circuits</i> ; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; October 1997; Pages 1173-1185; Vol 16, No. 10			
	14	VARIYAM, ET AL.; <i>Digital-Compatible BIST for Analog Circuits Using Transient Response Sampling</i> ; IEEE Design & Best of Computers; July-September 2000; Pages 106-115;			
	15	HOOKE, ET AL.; <i>"Direct Search" Solution of Numerical and Statistical Problems</i> ; May 1960, revised October 1960; Pages 212-229; Westinghouse Research Laboratories; Pittsburgh, Pennsylvania			
	16	Copy of Search Report for International Application No. PCT/GB03/02599 completed April 20, 2004			
	17	Copy of International Preliminary Examination Report for International Application No. PCT/GB03/02599 completed November 2, 2004			

Examiner Signature		Date Considered	
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